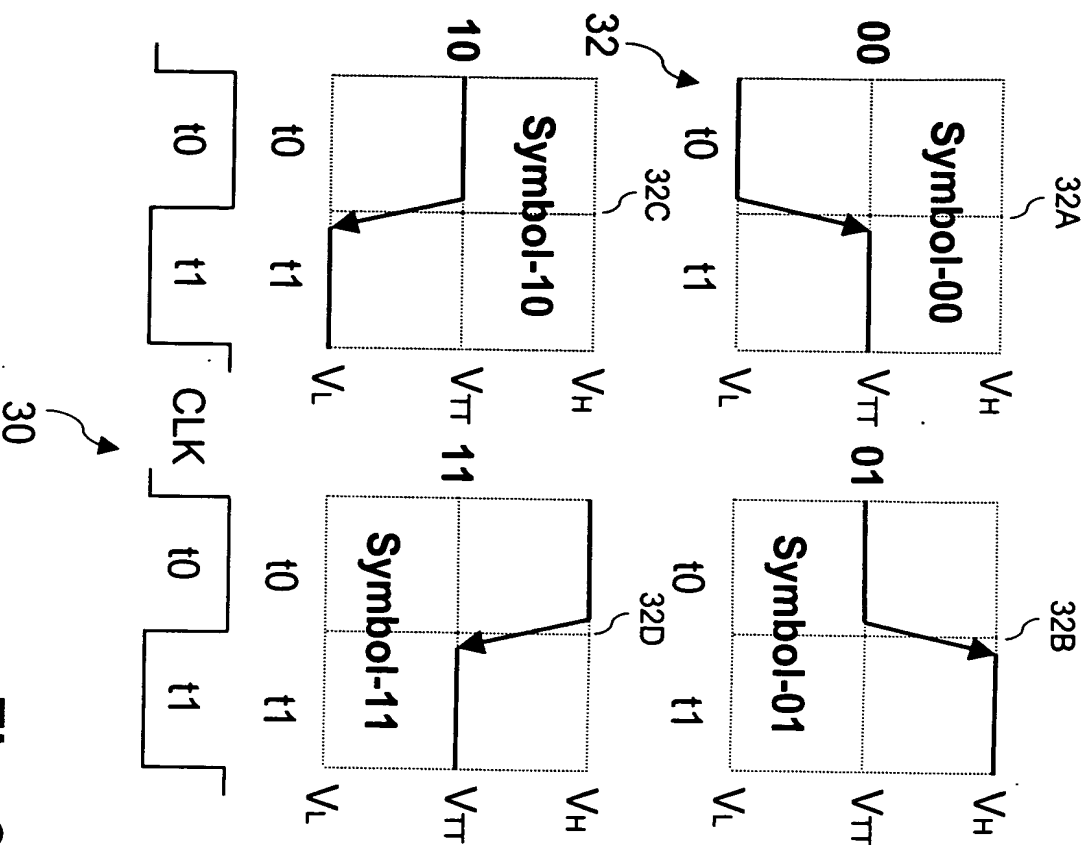


Fig. 1

Multi-Symbol Signaling Technique



D1	D0	Transition	Region	Symbol
0	0	Rising	Lower	Symbol-00
0	1	Rising	Upper	Symbol-01
1	0	Falling	Lower	Symbol-10
1	1	Falling	Upper	Symbol-11

		t_0 CLK=high	t_1 CLK=low	
D1	D0			Symbol
0	0	V_L	V_{TT}	Symbol-00
0	1	V_{TT}	V_H	Symbol-01
1	0	V_{TT}	V_L	Symbol-10
1	1	V_H	V_{TT}	Symbol-11

Fig. 2

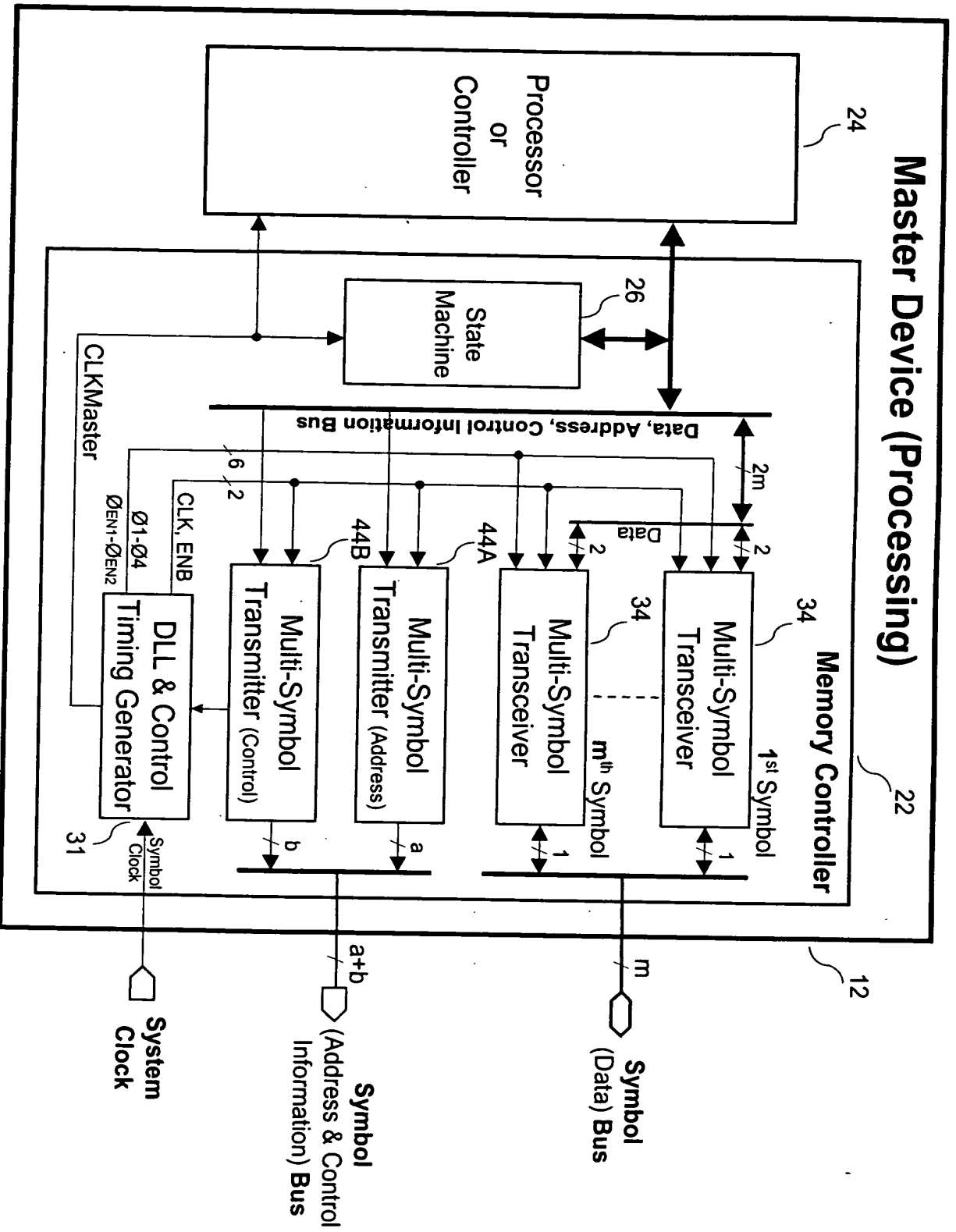


Fig. 3

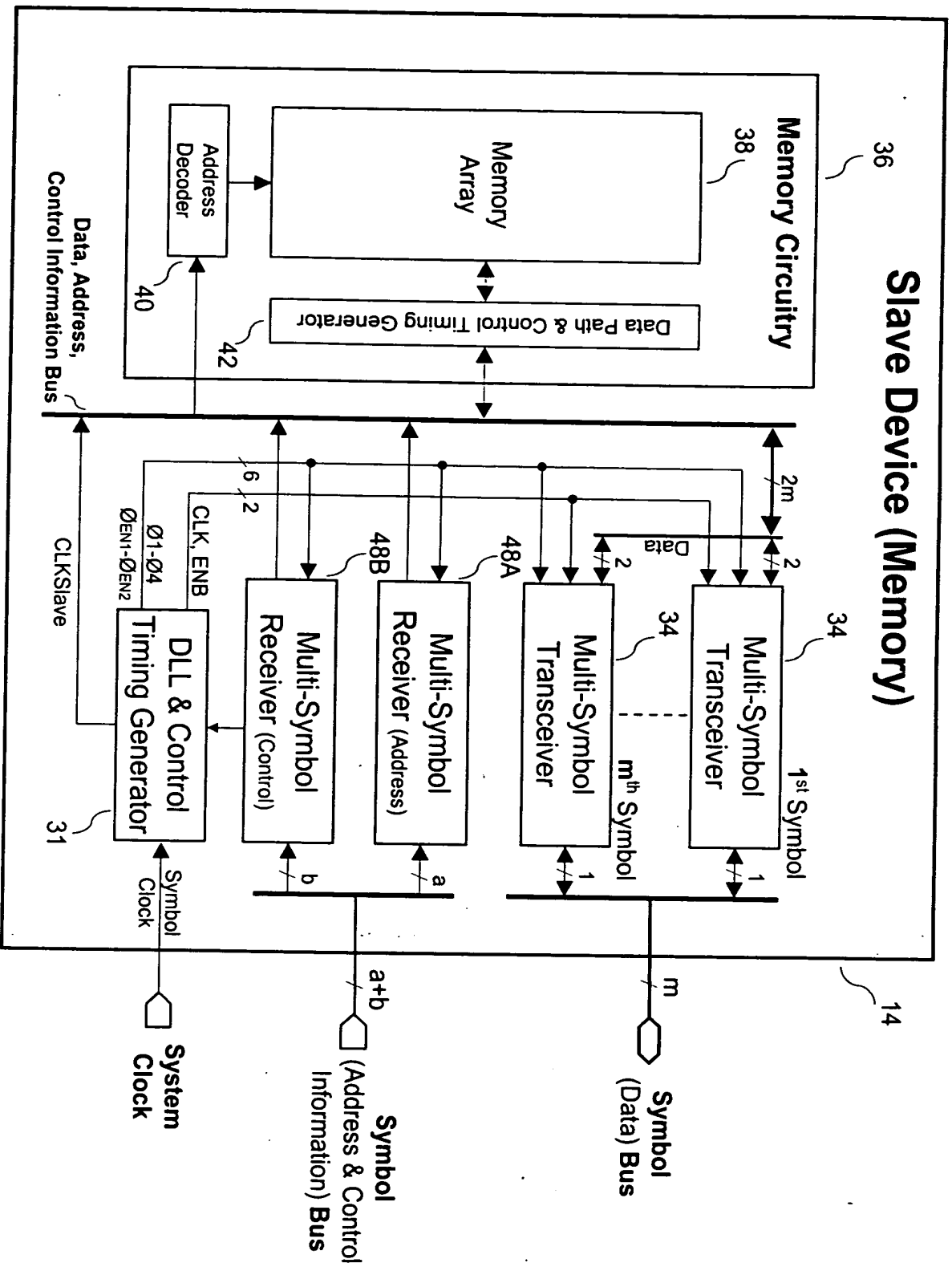


Fig. 4

Multi-Symbol Transceiver

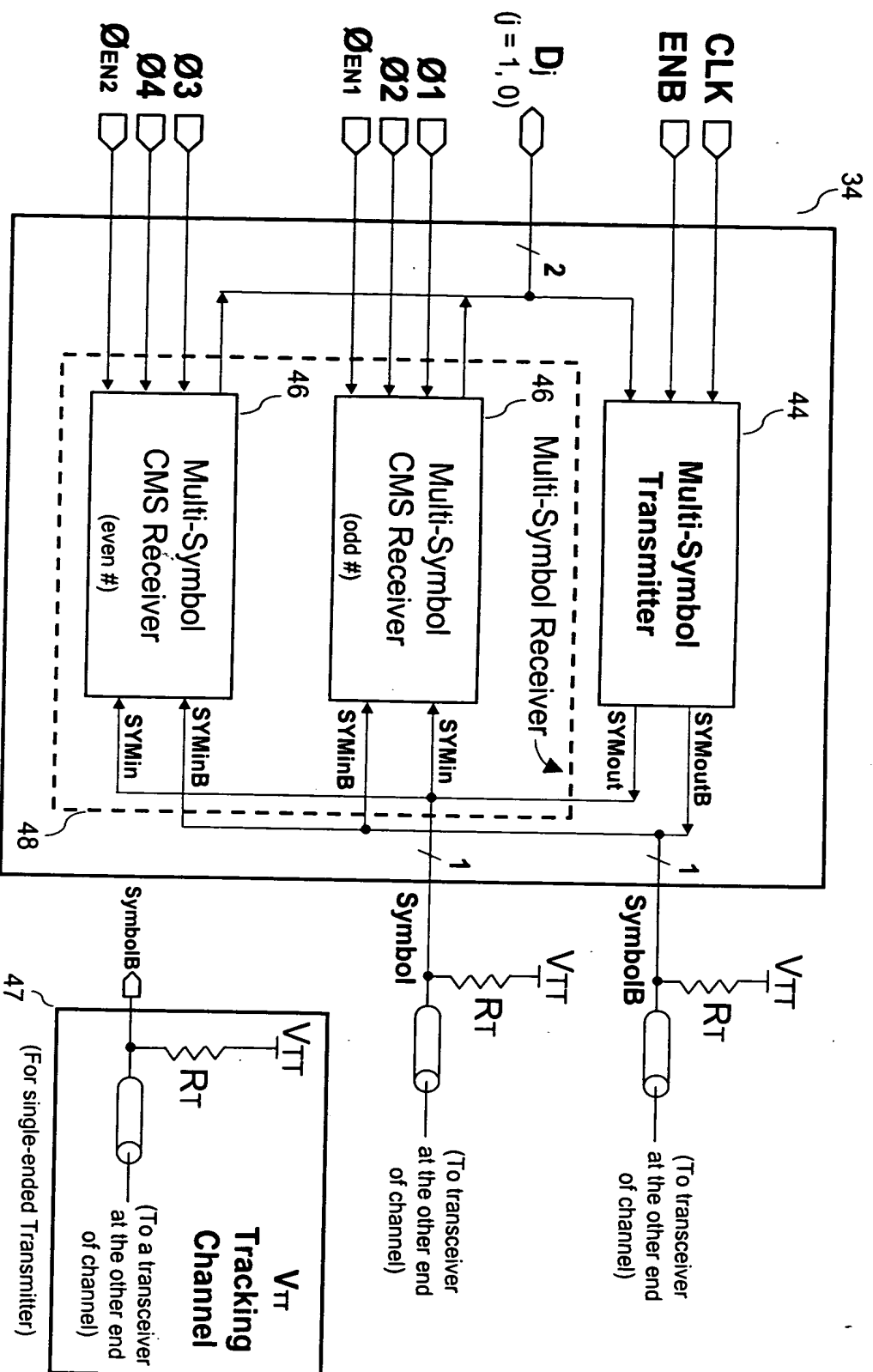


Fig. 5

Figure 1 illustrates a Multi-Symbol Transmitter and its timing characteristics.

Multi-Symbol Transmitter (44):

- The transmitter includes an **Output DC Level Calibration Circuit (52)** which receives a **CLK** signal and provides a reference signal to the differential output stage.
- A **Supply Source (55)** provides current to the differential pair (51, 53).
- The differential pair (51, 53) produces the output signals **ØPE** and **ØNE**.
- A **Driver Strength Control Circuit (54)** provides biasing signals (**ØP**, **ØN**, **NL**) and data signals (**do1**, **do0**) to the **Multi-Symbol Encoder Circuit (56)**.
- The **Multi-Symbol Encoder Circuit (56)** also receives **ENB** and **CLK** signals.
- The encoder output is connected to a **Bus (62)** via a driver (59).
- A feedback path (81, 83, 85) is also shown.

Symbol Timing Diagram (44):

- The diagram shows a bus with a resistor R_T connected to V_{TT} .
- It illustrates the timing of a **Symbol (m)** and its relationship to **Slave Device-1** and **Slave Device-k**.
- The timing parameters t_0 (CLK=high) and t_1 (CLK=low) are indicated.

	D1	D0	t_0 CLK=high	t_1 CLK=low
0	0	0	V_L	V_{TT}
0	1	1	V_{TT}	V_H
1	0	0	V_{TT}	V_L
1	1	1	V_H	V_{TT}

	t_0 CLK=high	t_1 CLK=low
D1	D0	
0	0	V_L
0	1	V_{TT}
1	0	V_L
1	1	V_H

Multi-Symbol Transmitter (differential)

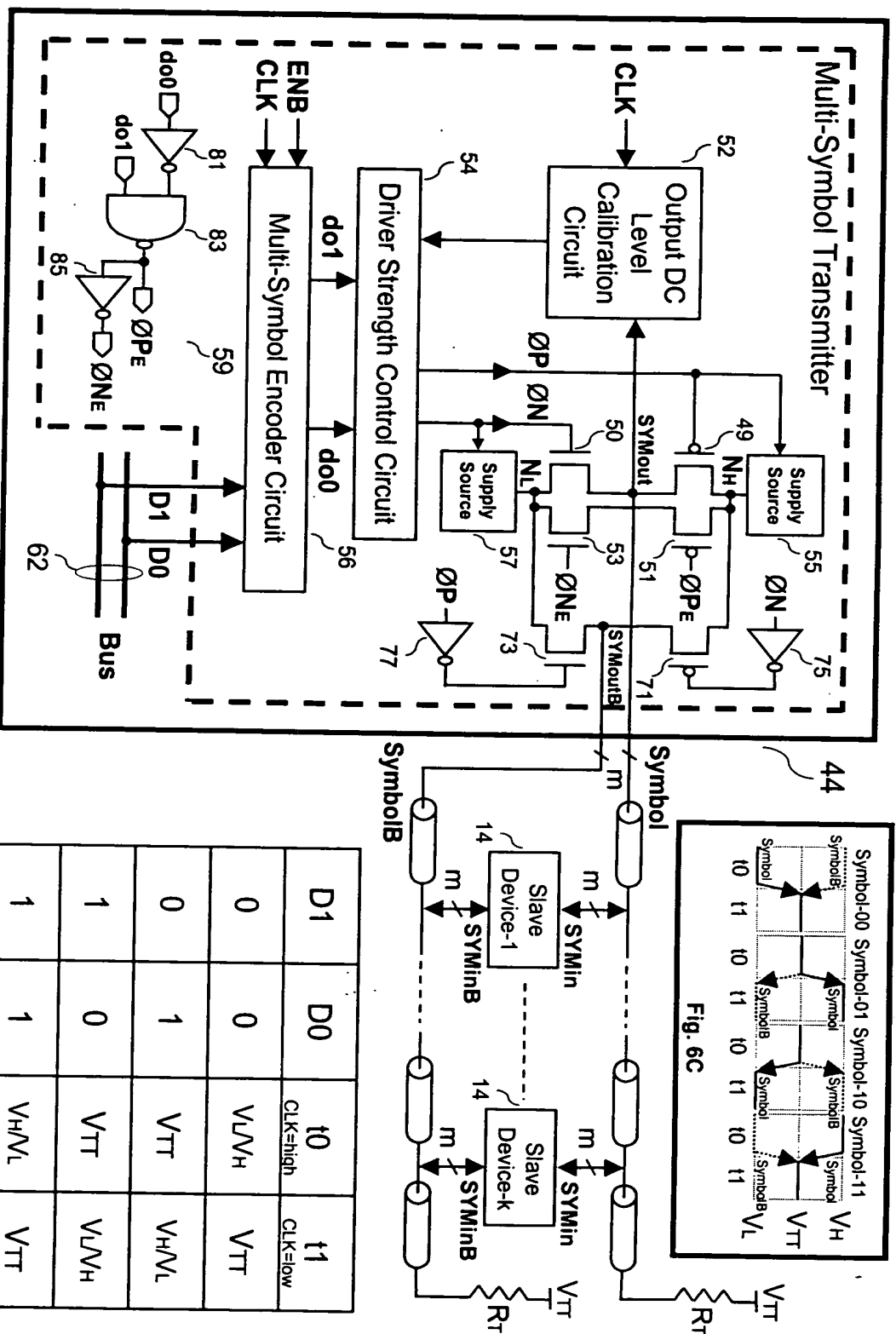
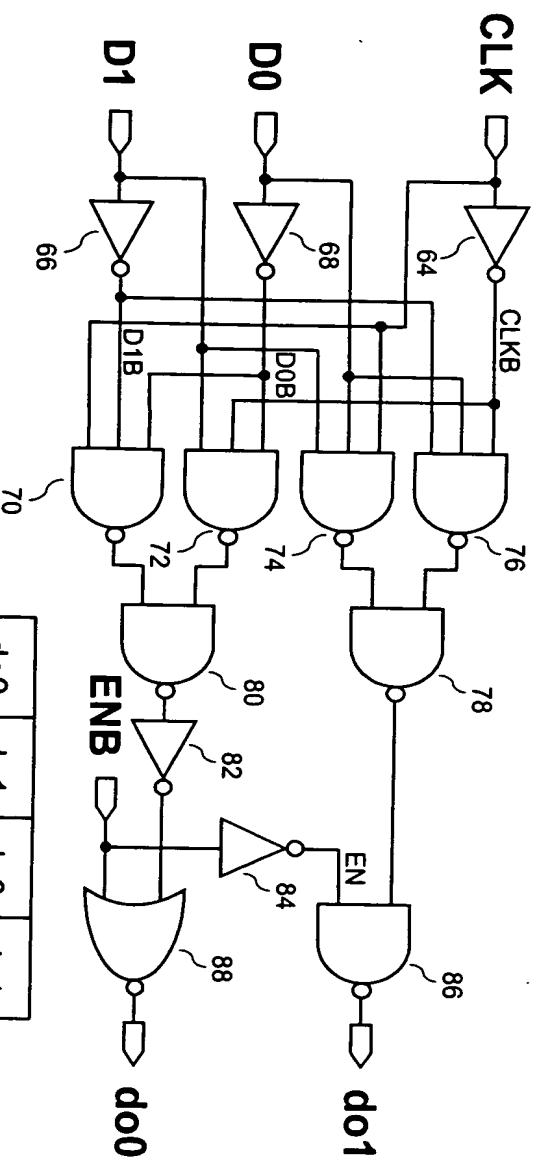


Fig. 6B

Multi-Symbol Encoder



				70			
				do0	do1	do0	do1
D1	D0	t_0 CLK=high	t_1 CLK=low	t_0 CLK=high	t_0 CLK=high	t_1 CLK=low	t_1 CLK=low
0	0	V_L	V_{TT}	1	1	0	1
0	1	V_{TT}	V_H	0	1	0	0
1	0	V_{TT}	V_L	0	1	1	1
1	1	V_H	V_{TT}	0	0	0	1

Fig. 7

[illegible]

[illegible][illegible]

Multi-Symbol CMS Receiver

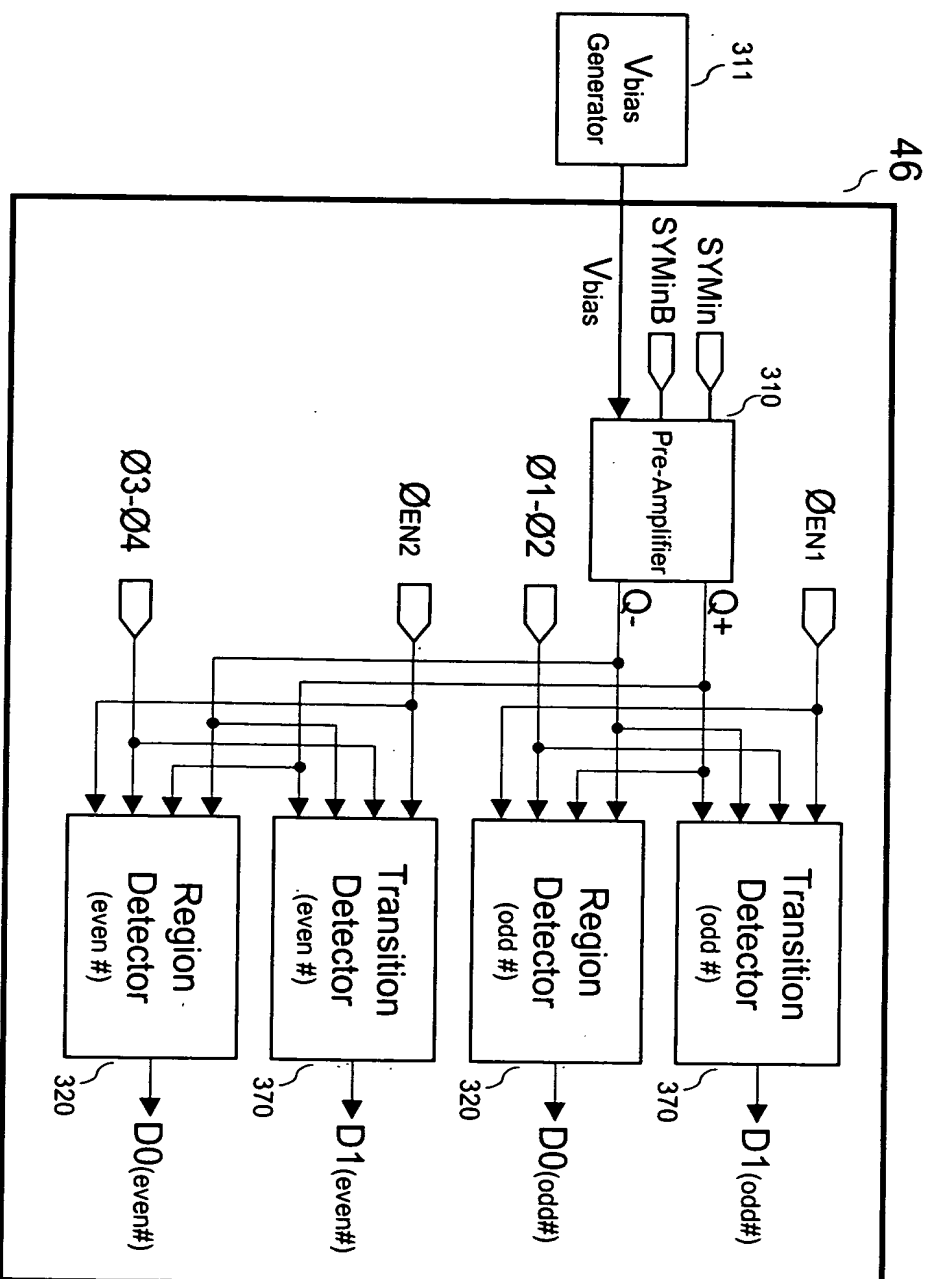


Fig. 9

Pre-Amplifier

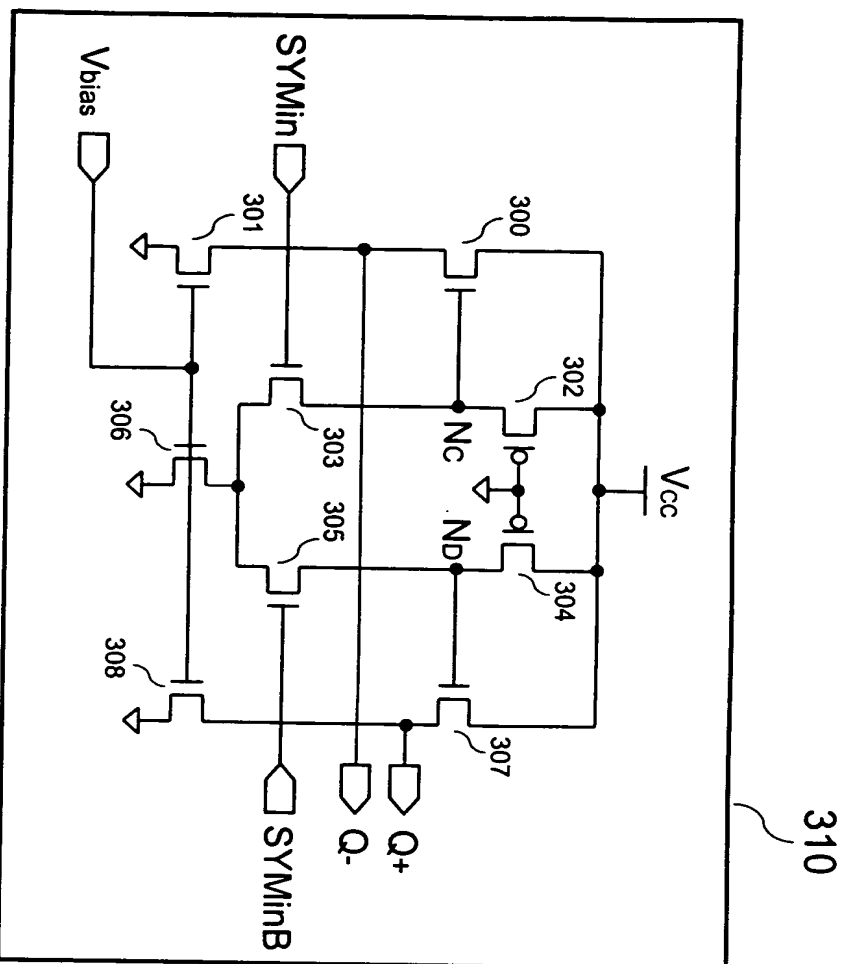
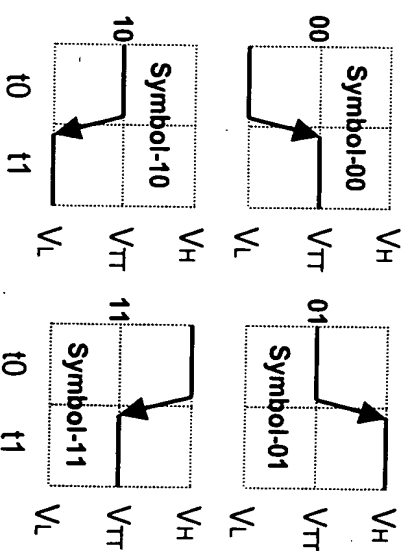
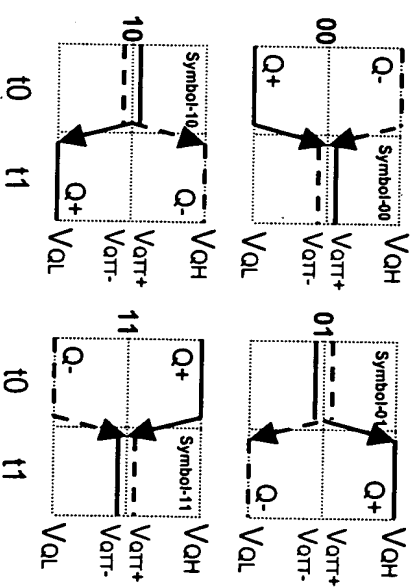


Fig. 10



[SYMin Waveforms]



[Q+/Q- Waveforms]

Transition Detector

Fig. 11A

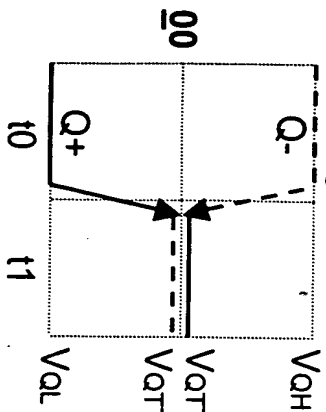


Fig. 11B

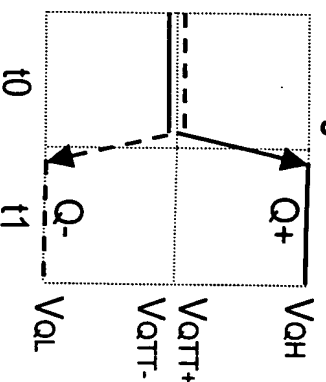


Fig. 11C

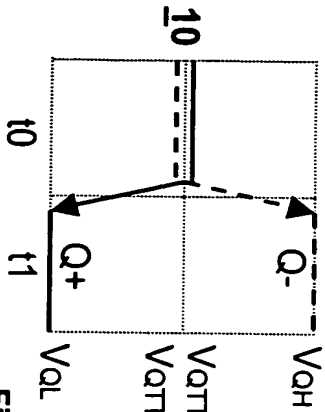


Fig. 11D

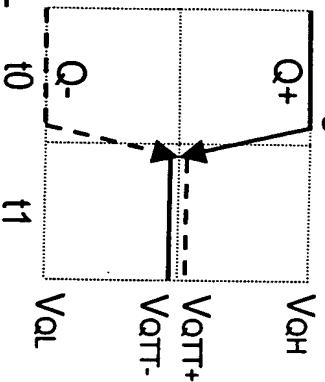


Fig. 11E

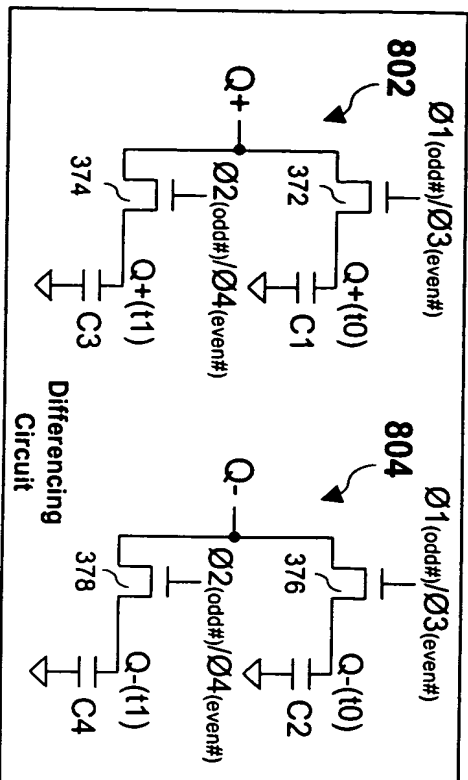


Fig. 11F

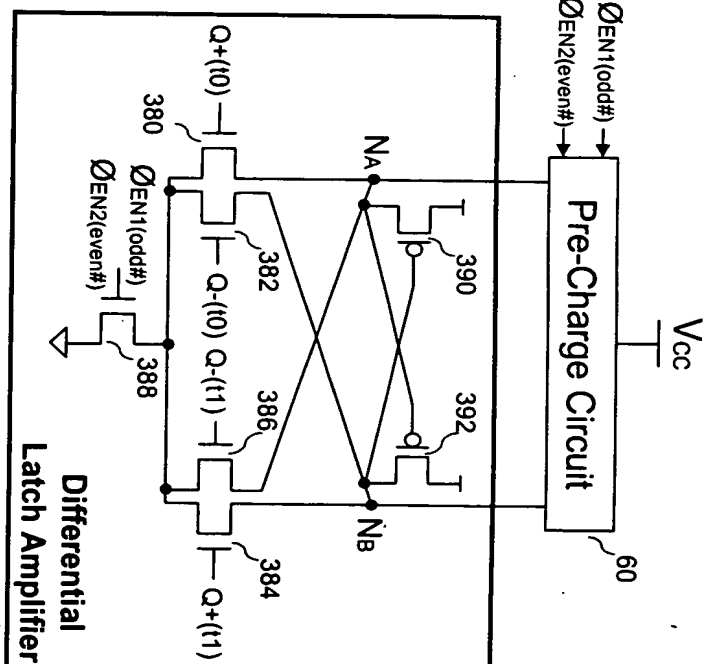
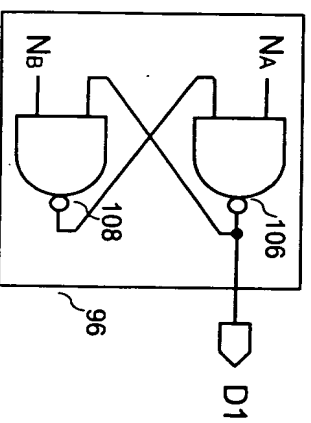


Fig. 11G



Region Detector

Fig. 12A

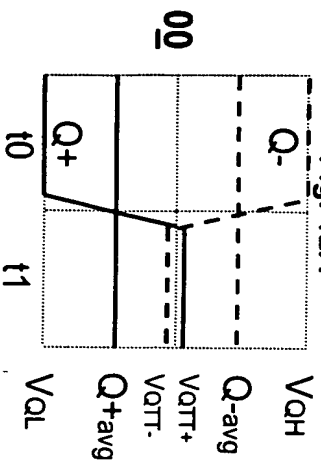


Fig. 12C

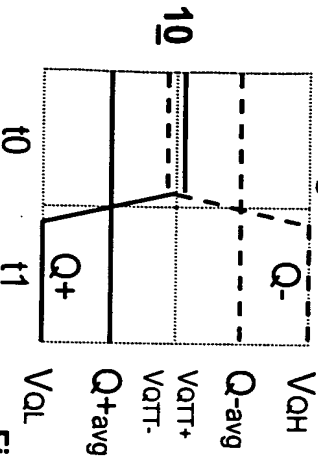


Fig. 12B

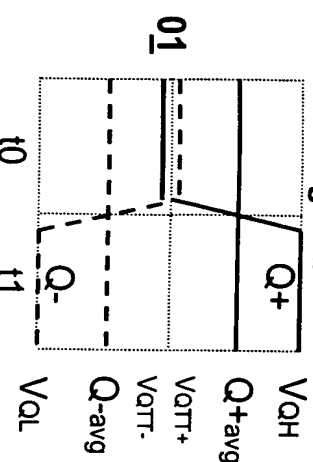


Fig. 12D

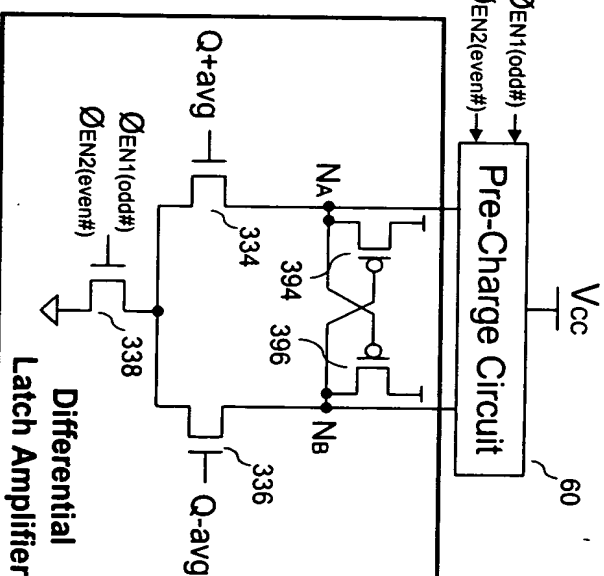
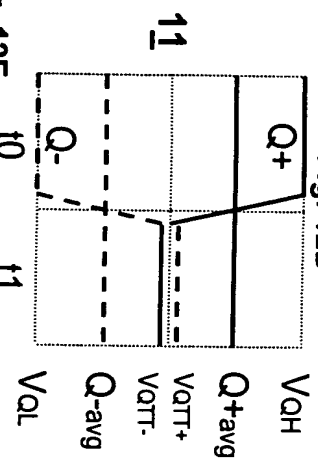


Fig. 12F

130

128

Hold Circuit

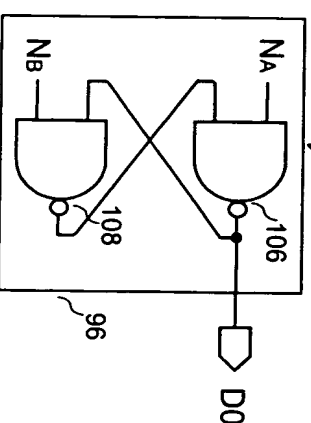
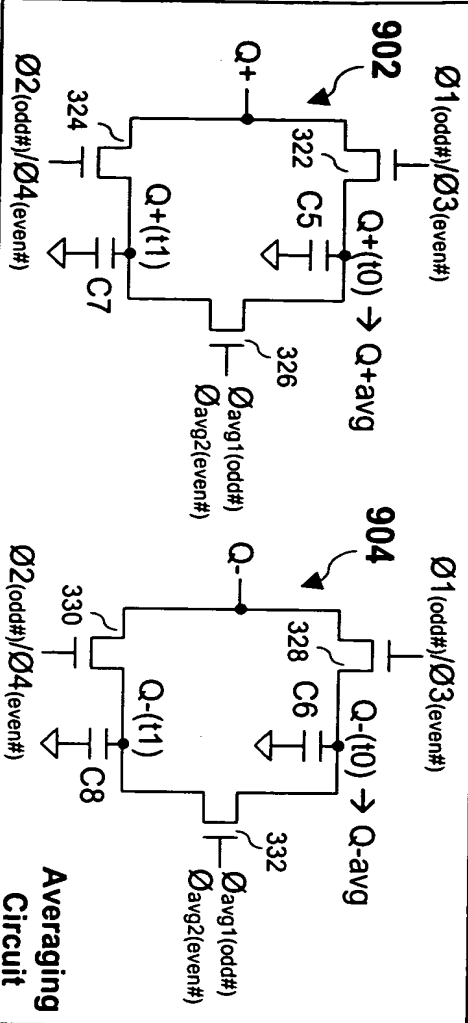


Fig. 12G



Averaging Circuit

Pre-Charge Circuit

60

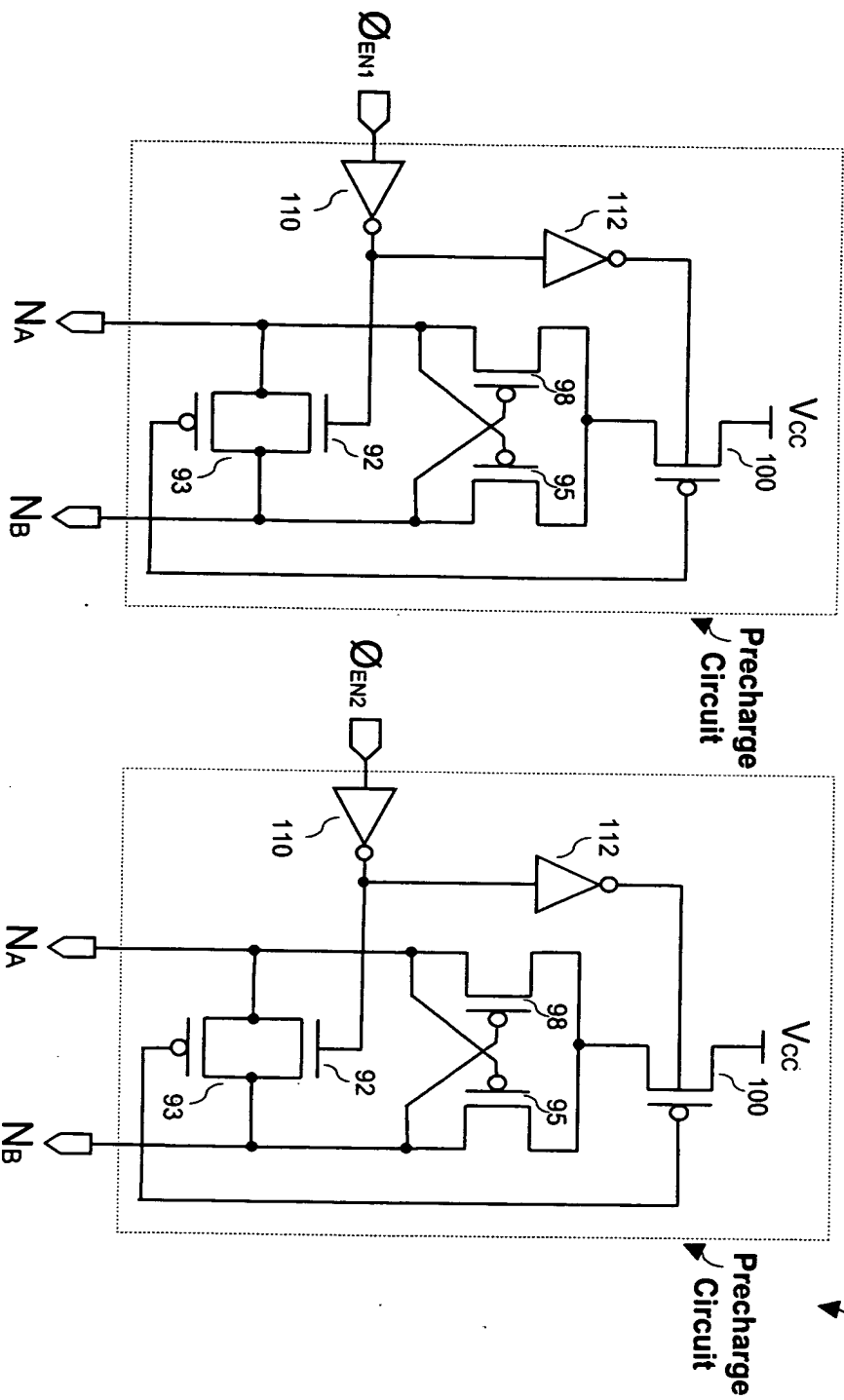


Fig. 13

Multi-Symbol Transfer Control Timings

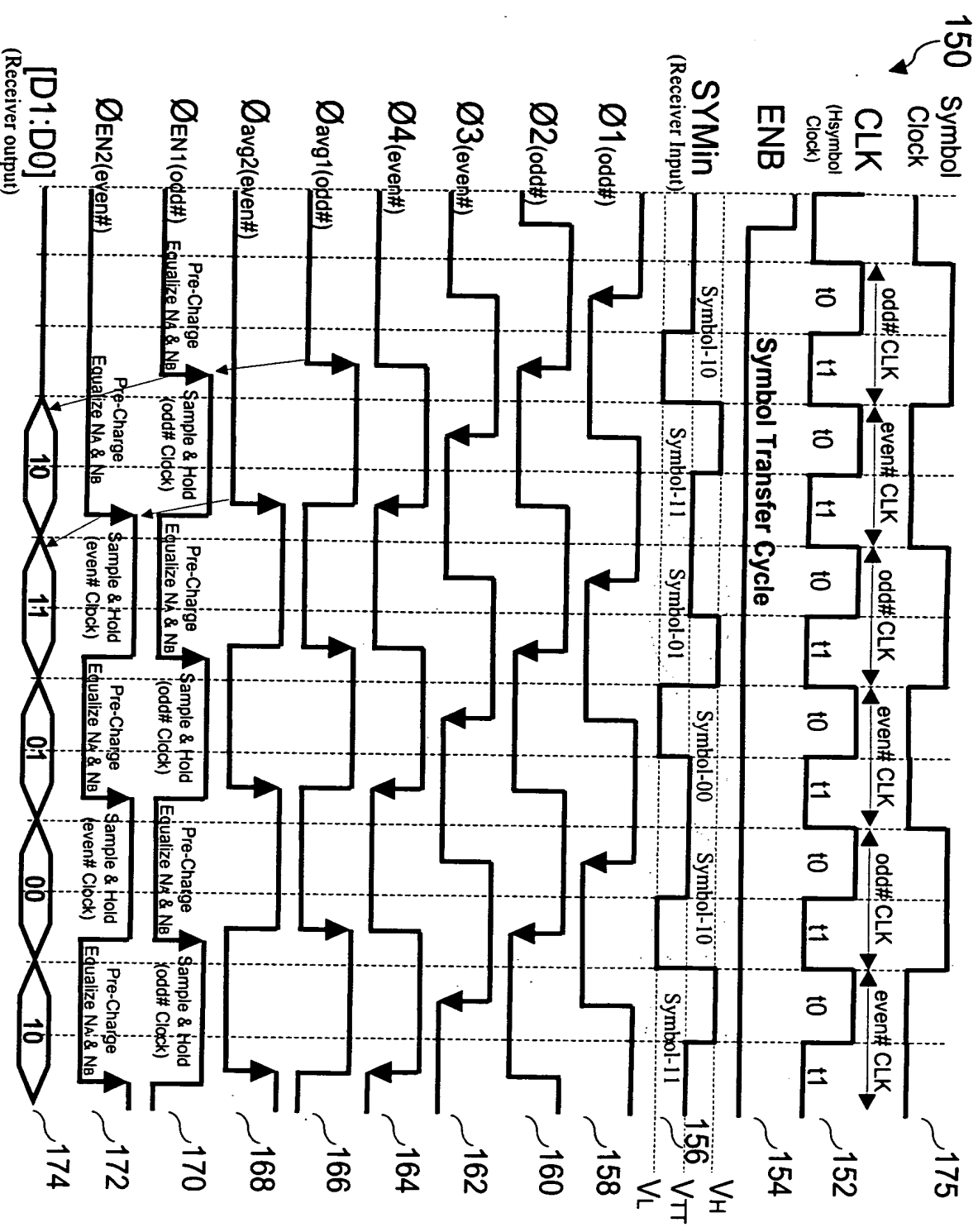


Fig. 14

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